10.2 A Highly Integrated 60GHz CMOS Front-End Receiver

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With the availability of 7GHz of unlicensed spectrum around 60GHz, there is a growing interest in using this resource for a host of new wireless consumer applications that require very high data rates. In order to achieve widespread adoption, it is highly desirable to implement mm-wave circuits in the lowest-cost technology — namely, CMOS. Recently published results in [1][2] have shown that 0.13µm CMOS has sufficient performance to be used for an integrated radio solution at 60GHz.

This paper describes a highly integrated 60GHz CMOS receiver front-end consisting of an LNA, a quadrature balanced downconverting mixer, a 30GHz VCO, and a frequency doubler, as shown in Fig. 10.2.1. Individual circuit blocks are also fabricated to characterize their performance separately. The front-end is fabricated in a 1P6M 0.13µm standard digital CMOS process, with a substrate resistivity of 10Ω-cm. Transit frequency (f_T) and maximum frequency of oscillation (f_{max}) of 85GHz and 135GHz, respectively, have been reported for NMOS devices in this process [1]. To predict the mm-wave behavior of CMOS transistors, large-signal BSIM3 transistor models with external parasitics are extracted prior to the design of the circuits [4].

The LNA topology consists of 3 cascade stages with input, output, and interstage reactive matching, as shown in Fig. 10.2.2. Cascode transistors, used in order to reduce the Miller capacitance and improve stability, have a maximum available gain of 6.0dB at 60GHz at a current density of 150µA/µm. Coplanar wave-guide (CPW) transmission lines are used extensively in the design of impedance matching networks, interconnect wiring, and bias networks. All CPW lines are kept as short as possible to minimize losses. A standalone version of the LNA (with pads), matched to the off-chip 50Ω interface, is implemented and measured separately [1]. It achieves a peak power gain of 12dB, input and output return losses >15dB, and its 3dB bandwidth is from 51 to 65GHz. The measured reverse isolation is better than 45dB up to 65GHz. The NF is 8.8dB at 60GHz and remains below 9.3dB up to 63GHz. Since the integrated LNA output does not need to drive a pad or be matched to an off-chip 50Ω load, it is matched directly to the input of the quadrature mixer, and therefore, it provides a higher performance compared to the standalone version.

The quadrature balanced downconverting mixer consisting of two unit single-gate mixers and a 90° branch-line hybrid, is shown in Fig. 10.2.3. The mixer is designed to downconvert from the nominal RF frequency of 60GHz to an IF of 2GHz using a 58GHz, 0dBm LO. By taking advantage of the intrinsic device capacitances, it is possible to provide the required 90° phase shift by using CPW transmission lines shorter than λ/8. The LO and RF matching networks are co-designed with the 90° branch-line hybrid and gate-bias network to further minimize the length of the transmission lines and therefore reduce the insertion loss of the input passive circuit. The IF matching network at the drain consists of on-chip lumped LC components. It provides matching at the 2GHz IF as well as filtering of the LO and RF. A standalone version of the mixer (with pads), matched to the off-chip 50Ω LO and RF interface, is fabricated and characterized separately [3]. The mixer has a measured conversion loss of better than 2dB at 60GHz (0dBm LO power), and a 3dB RF bandwidth of 6.1GHz. The SSB noise figure is 13.8dB at 60GHz. The input-referred 1dB compression point of the mixer is –3.5dBm. The mixer draws 2mA from a 1.2V supply.

The simplified schematic of the 3-stage frequency doubler is shown in Fig. 10.2.4. It consists of a 30GHz input driver, the multiplier core, and the 60GHz LO buffer. Cascode devices with input, output, and interstage reactive matching are used to implement the input driver and output buffer stages. The frequency doubling stage is based on a common-source NMOS transistor biased close to its threshold voltage to efficiently generate the second harmonic component of the input. A passive network at the drain of the transistor rejects the 30GHz fundamental, maximizes the generation of the second harmonic at 60GHz, and optimizes the power transfer to the output buffer.

A standalone version of the doubler, matched to a 50Ω input (at 30GHz) and a 50Ω output (at 60GHz), is implemented and characterized separately. A conversion gain of 7.2dB at 58GHz is achieved with a –6dBm, 29GHz input signal. The 3dB bandwidth at this input power level is from 53GHz to 62.5GHz. The fundamental frequency component at the output of the doubler is below –35dBc. The doubler alone draws 2mA while the input and output stages draw 8mA and 12mA, respectively.

Both standalone and integrated versions of a 28.4-29.4GHz Pierce VCO are implemented. The standalone implementation of the VCO provides –3dBm output power to a 50Ω load at 29GHz with a phase noise of –93dBc/Hz at 1MHz offset. The integrated version of the VCO and the doubler provides 2dBm output power at 58GHz with a measured phase noise of –86dBc/Hz at 1MHz offset.

Figure 10.2.5 shows the die micrograph of the integrated front-end. The chip area is about 3.8mm^2 including pads. On-wafer measurements are performed using Cascade Microtech Infinity probes. An Anritsu 37397C VNA is used for S-parameter measurements. The input return loss at the RF port is better than 15dB. Figure 10.2.6 shows the conversion characteristics of the front-end with conversion gain of 11.8dB at 60GHz. The RF and LO frequencies are varied to obtain the frequency characteristics of the mixer for fixed IF frequency of 2GHz. To obtain a broadband frequency characteristic, another fabricated version of the front-end with an external 30GHz LO is used. As shown in Fig. 10.2.6, the 3dB RF bandwidth of the mixer is about 6GHz. The measured input-referred 1dB compression point of the front-end is –15.8dBm at 60GHz. Noise figure measurement of the integrated front-end is performed using a NoiseCom WR-15 noise source, WR-15 waveguide probes, and an Agilent N8973A NF measurement system. The measured NF of the downconverter is also shown in Fig. 10.2.6. The NF is 10.4dB at 60GHz. The integrated front-end draws 64mA from a 1.2V supply.

Acknowledgment:
This work is funded by the DARPA TEAM project and the Berkeley Wireless Research Center sponsoring companies. The authors thank STMicroelectronics for chip fabrication and J. Tani and P. McElwee for useful discussions.

References:
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[3] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A 60-GHz Down-Converting CMOS Single-Gate Mixer," *RFIC Symp. Dig. Papers*, pp. 163-166, June, 2005.
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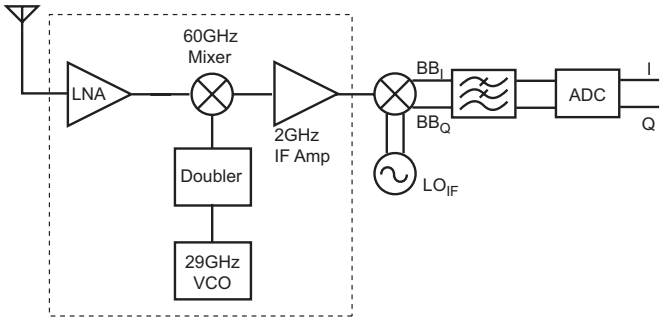

Figure 10.2.1: Block diagram of the 60GHz receiver. Dashed box shows the integrated CMOS front-end.

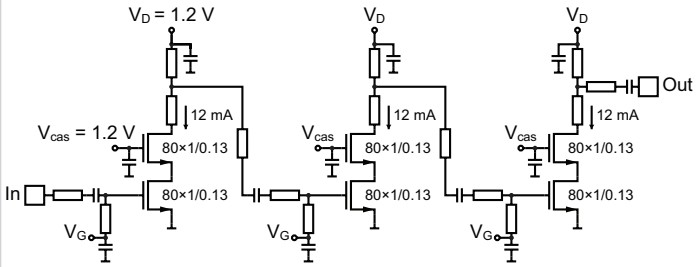

Figure 10.2.2: Schematic of the 3-stage 60GHz LNA.

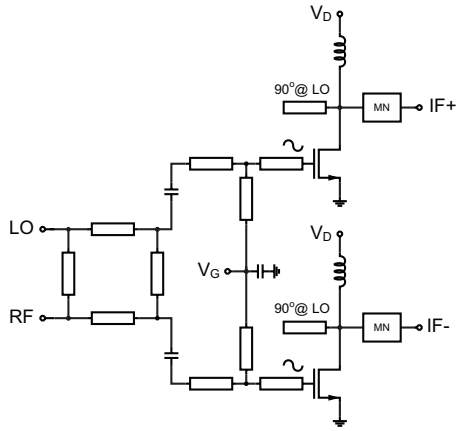

Figure 10.2.3: Simplified circuit diagram of the single-gate quadrature balanced mixer.

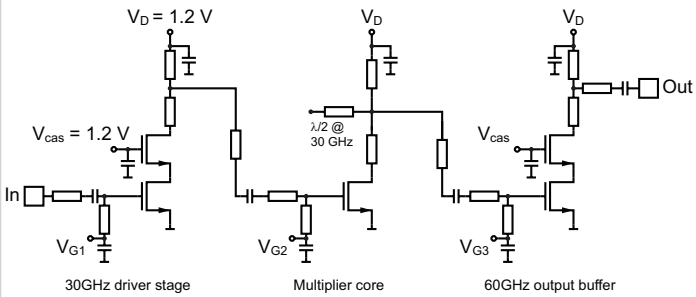

Figure 10.2.4: Simplified circuit diagram of the frequency doubler.

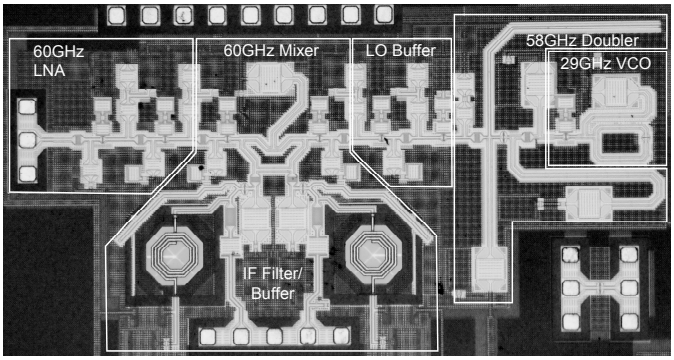

Figure 10.2.5: Die micrograph of the integrated receiver front-end.

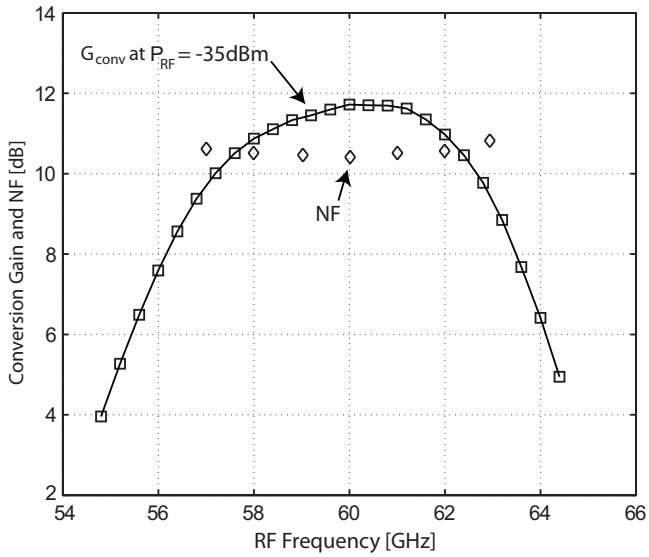

Figure 10.2.6: Measured conversion gain and noise figure of the integrated front-end.